REMARKS

The applicants appreciate the Examiner's thorough examination of the Application and request reexamination and reconsideration of the Application in view of the following remarks.

The subject invention results from the realization that, in a feedback system where the output closely tracks the input, the error signal is small, and so rather than sample both the input and feedback signals before taking the difference to create the error signal, it is better to form the error signal with a continuous-time (non-sampling) circuit followed by a gain stage and then sample this amplified error signal using a switched-capacitor circuit. This novel arrangement causes the input-referenced switch thermal noise to be reduced by the amount of the gain used in the error path. The amount of gain that can be used in the error path depends on how closely the output tracks the input; it is desirable to make this gain as large as possible without causing the error signal to exceed the supply voltage.

Claims 4-6, 9 and 10 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,304,608 to Chen et al. in view of U.S. Patent No. 5,805,093 to Heikkilä et al. The Examiner notes that this rejection is a multiple reference 35 U.S.C. §102 rejection. In particular, the Examiner alleges that Heikkilä et al. shows that a sampling capacitor and switch, which are not disclosed in the Chen et al. reference, are inherent in an integrator used in an analog to digital conversion system.

Chen et al. shows a multi-bit sigma-delta converter that includes, as shown in Fig. 2, a loop filter 22, an N-level quantizer 25, element selection logic 26, and an N-level digital to analog converter (DAC) 27. The Examiner alleges that loop filter 22 includes an amplifying means g1 for amplifying a different signal. However, Fig. 6 of Chen et al., which shows the N-level DAC 60 together with the integrator 53, does not show an amplifier before an input sampling capacitor

and a switch. G1, which the Examiner asserts is an amplifier, is in actuality part of DAC 60 or part of integrator 53 which is after switch 50. Thus, Chen et al. does not disclose or suggest a sigma-delta modulator having an input circuit including means for amplifying a different signal representative of the difference between an input signal and a quantized feedback signal and a filter circuit including at least an input sampling capacitor and switch which introduces thermal noise. As the Examiner will note, Chen et al. also does not disclose or suggest reducing the input-referred thermal noise by a factor of approximately the gain of the amplification because Chen et al. does not disclose an amplifier before a switch.

The subject invention as claimed includes an input circuit that includes either means for amplifying a difference signal representing the difference between an input signal and a quantized feedback signal or a summing circuit for providing a difference signal and an amplifier for amplifying the difference signal. One means for amplifying the difference signal is amplifier 40 as shown in Figs. 1 and 2 of the subject application. Another is summing amplifier 11A as shown in Fig. 3 of the subject application. Chen et al. does not disclose or suggest either a means for amplifying the difference signal or an amplifier for amplifying the difference signal because g1, which the Examiner asserts is an amplifier, is in actuality part of DAC 60 or part of integrator 53 which is after switch 50.

In contrast to Chen et al., claim 4 of the subject application recites: "A $\Sigma\Delta$ modulator with a filter system having reduced switch thermal noise comprising: an input circuit for receiving an input signal and a quantized feedback signal and providing a signal representative of the difference; a filter circuit including at least an input sampling capacitor and switch which introduces thermal noise error; a quantizer circuit for quantizing the output of said filter circuit; a feedback circuit, responsive to said quantizer circuit, for delivering to said input circuit said

quantized feedback signal; and said input circuit including means for amplifying said difference signal, before it is submitted to said filter circuit to reduce the input-referred thermal noise by a factor of approximately the gain of the amplification" (emphasis added). Chen et al. does not disclose a means for amplifying the difference signal before it is submitted to a filter circuit.

Also in contrast to Chen et al., claim 9 of the subject application recites: "A ΣΔ modulator with a filter system having reduced switch thermal noise comprising: a summing circuit for receiving an input signal and a quantized feedback signal and providing a signal representative of the difference; a filter circuit including at least an input sampling capacitor and switch which introduces thermal noise error; a quantizer circuit for quantizing the output of said filter circuit; a feedback circuit, responsive to said quantizer circuit, for delivering to said summing circuit said quantized feedback signal; and an amplifier circuit for amplifying said difference signal, before it is submitted to said filter circuit to reduce the input-referred thermal noise by a factor of approximately the gain of said amplifier circuit". Chen et al. also does not disclose an amplifier circuit for amplifying the difference signal between the input signal and a quantized feedback signal.

The Examiner alleges that Heikkilä et al. overcomes the deficiencies of Chen et al. because it allegedly shows that a switching circuit is inherently a part of a sigma-delta modulating system. However, despite that Heikkilä et al. shows a switching system in Fig. 2, the combination of Heikkilä et al. and Chen et al. actually teaches away from the subject invention. In particular, Fig. 1 of Heikkilä et al. shows "scaling means" 17 which is shown in greater detail as a switching system in Fig. 2. Thus, Heikkilä et al. in actuality teaches to those of ordinary skill in the art that a scaling means is a switching system, rather than an amplifier, which further supports Applicants' arguments above that g1 of Chen et al. is not an amplifier. In other words, Heikkilä et al. teaches

that g1 of Chen et al. is part of a switching system rather than a means for amplifying or an amplifier as the Examiner asserts. Thus, the combination of Chen et al. and Heikkilä et al. not only does not produce the subject invention, it actually teaches away from the subject invention.

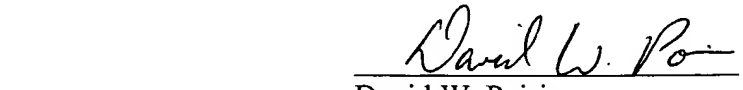
Finally, as Applicants' stated in their last Response dated July 8, 2003, Chen et al. does not disclose or suggest either an input circuit or a summing circuit for receiving an input signal and a quantized feedback signal. Although Chen et al. shows an N-level quantizer 25, the output of quantizer 25 is applied to a digital to analog converter 27 which has an output that is applied to a summing circuit 21. Thus, Chen et al. does not disclose or suggest an input circuit or summing circuit that receives a quantized feedback signal because N-level DAC 27 provides an analog output signal which is applied to summing circuit 21.

Accordingly Chen et al. and Heikkilä et al., either alone or in combination, do not disclose or suggest the subject invention as claimed. Applicants respectfully request that the Examiner withdraw the rejections under 35 U.S.C. §102(e).

Each of the Examiner's rejections has been addressed or traversed. Accordingly, it is respectfully submitted that the application is in condition for allowance. Early and favorable action is respectfully requested.

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,



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